DOI 10.31489/2023No4/74-80

UDC 53.08

IMPLEMENTATION OF FUNCTIONAL BLOCK RADIO UNIT BASED ON SYSTEM-ON-CHIP

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This article discusses the implementation of the Radio Unit functional block based on the System-on-Chip. The primary focus was on integrating Radio Unit blocks such as modulation and Fast Fourier Transform on Field-Programmable Gate Array. Technical aspects of design, module testing, and Radio Unit block performance optimization are thoroughly examined. The results demonstrate that when separating the functionality of the 7.3 technology Fifth Generation (5G) radio block, the modulation module uses the minimum Field-Programmable Gate Array resources compared to other blocks. The Fast Fourier Transform block can meet delay requirements at the maximum Field-Programmable Gate Array size and clock frequency of 250 MHz. This article serves as a resource for engineers and researchers interested in optimizing the development and integration process of high-performance functional blocks in modern radio systems.

Keywords*:* Field-Programmable Gate Array, Zynq, Fifth Generation New Radio, Radio Unit, Orthogonal Frequency-Division Multiple Access.

1. Introduction

5G (Fifth Generation) technology is transitioning from promise to reality in mobile communication, playing a crucial role in ensuring outstanding performance and ultra-reliable communication services. This article focuses on research efforts aimed at implementing 5G technology, with a particular emphasis on the use of Field-Programmable Gate Arrays (FPGAs) in this exciting context. Today, the challenge is not only to provide uninterrupted connectivity in the face of society's growing dependence on data transmission but also to meet the increasing demand for higher data transfer speeds and service reliability. In this regard, 5G emerges as a kind of backbone, opening new horizons in the realm of mobile communications.

The investigation of the architectural framework of this state-of-the-art technology precedes the exploration of the role of FPGAs in the implementation of 5G. The organizational structure of the 5G network revolves around three distinct functional blocks, namely the Centralized Unit (CU), Distributed Unit (DU), and Radio Unit (RU). Each of these blocks performs specific functions, ensuring synergy in the overall network operation. When designing RUs, critical considerations include size, weight, and power consumption. The efficiency of these parameters is essential to ensure the seamless operation of the network and, consequently, to create the best conditions for end-users.

FPGAs serve as a key tool in providing high-speed data processing in light of the aforementioned design requirements for RUs. The flexibility, energy efficiency, and parallel processing capabilities make FPGAs an ideal choice for the efficient implementation of 5G NR (New Radio) functions. As early as now, we witness the results of these studies in works [1-5], where the implementation of certain 5G NR functions on FPGAs is comprehensively described. This not only demonstrates the relevance of using FPGAs in this field but also underscores their ability to adapt to the requirements of high-speed data processing and parallel processing.

Thus, our article aims not only to uncover the fundamental aspects of designing RUs within 5G networks but also to conduct a detailed examination of the role of FPGAs in this context. The past years attest that FPGAs are not merely a theoretical proposition but a concrete tool that can effectively impact the development of key components of 5G technology. We will delve deeper into the influence of FPGAs on data transfer speed, power consumption, and overall reliability of 5G networks, opening new perspectives for the further advancement of mobile communications in the following sections of our article.

2. Statement of the problem

The work [6] provides a review of the current state of 5G technology, presenting fundamental concepts and explaining the construction of physical channels. Research by [7] suggests detailed descriptions of the functional division of the 5G network. It is demonstrated that performance optimization can be achieved through functional separation of 5G technology blocks.

Results of implementing the 5G DU Low-PHY function on SmartNIC based on FPGA are presented in the work [8]. Moreover, it is shown that FPGA-based implementations exhibit lower processing time and energy consumption compared to CPU-based implementations by up to two cores. The work [9] reveals that the research results of implementing the 5G-NR DU receiver based on Matlab/Simulink using HDL Coder are presented. Various constructive parameters are evaluated, including EVM, resource utilization, power, throughput, maximum operating frequency, and delay for different modulation schemes. There is a direct correlation between the type of input data and these constructive parameters, with the modulation scheme being practically independent of the model.

The research results on the implementation of a transceiver on FPGA for 5G PDSCH in the FR 28 GHz frequency band are presented in a study [10]. The Xilinx RFSoC platform and the Python Productivity for Zynq (PYNQ) software environment are utilized. The RFSoC platform is scalable to provide multiple T/R channels for high-speed data transmission and can be integrated with the active antenna array radio frequency subsystem to format the base radio unit (RU) of the O-RAN system.

The research results on the implementation of 5G-NR DU and RU on FPGA are outlined in an article by [11]. The 5G-NR DU receiver, combined with the RU receiver, was implemented in the ZCU102 evaluation kit with the integrated AD9371 transceiver. Resource utilization is at 25.7%, with 4.4% allocated to the 5G DU receiver and 21.3% to the AD9371 reference project, operating at a maximum frequency of 245.76 MHz [12] presents the implementation of a multimode DU transmission chain on FPGA. A comparative analysis of physical layer differences between 4G-LTE and 5G-NR mobile networks was conducted to determine fundamental changes in the architecture of each generation's DU. The FPGA implementation has an EVM of 0.24% for 4G and 1.60% for 5G.

Various applications of FPGA in the 5G network are presented in the work [13]. Several more works [14-16] are devoted to the implementing computational blocks of the 5G network on FPGA. Considering the aforementioned works, it is deemed advisable to conduct research on the implementation of physical radio modules of 5G technology on FPGA to reduce processing time with minimal energy consumption.

3. Methods

This study implemented a functional RU block based on FPGA. The transmitter-receiver processing module was realized on the ZedBoard evaluation kit with the AD-FMCOMMS3-EBZ board. ZedBoard is used for designing digital circuits using the programmable AMD Xilinx Zynq-7000 SoC. This device includes all the necessary interfaces for versatile applications. The data processing module of the RU block was developed and tested in the Vivado 2017.4 software environment using the Hardware Description Language (HDL) Verilog. There are several methods of functional partitioning for 5G networks [17-18]. Partitioning 7 is considered optimal in terms of simplicity and cost-effective RU design. Therefore, in this work, an RU block with functional partitioning 7 was implemented. However, there are several variants of partitioning 7.

Figure 1 illustrates these partitioning options for 5G networks. The partitionings 7.2 and 7.3 was chosen within the framework of this study.

4. Results and Discussion

The QPSK, 16QAM, 64QAM, and 256QAM modulators were implemented based on FPGA using the Verilog language. The modulation QPSK signal constellation is shown in Figure 2 for comparison with FPGA results. The results are shown in Figure 3 and are in complete accordance with the theoretical expectations.

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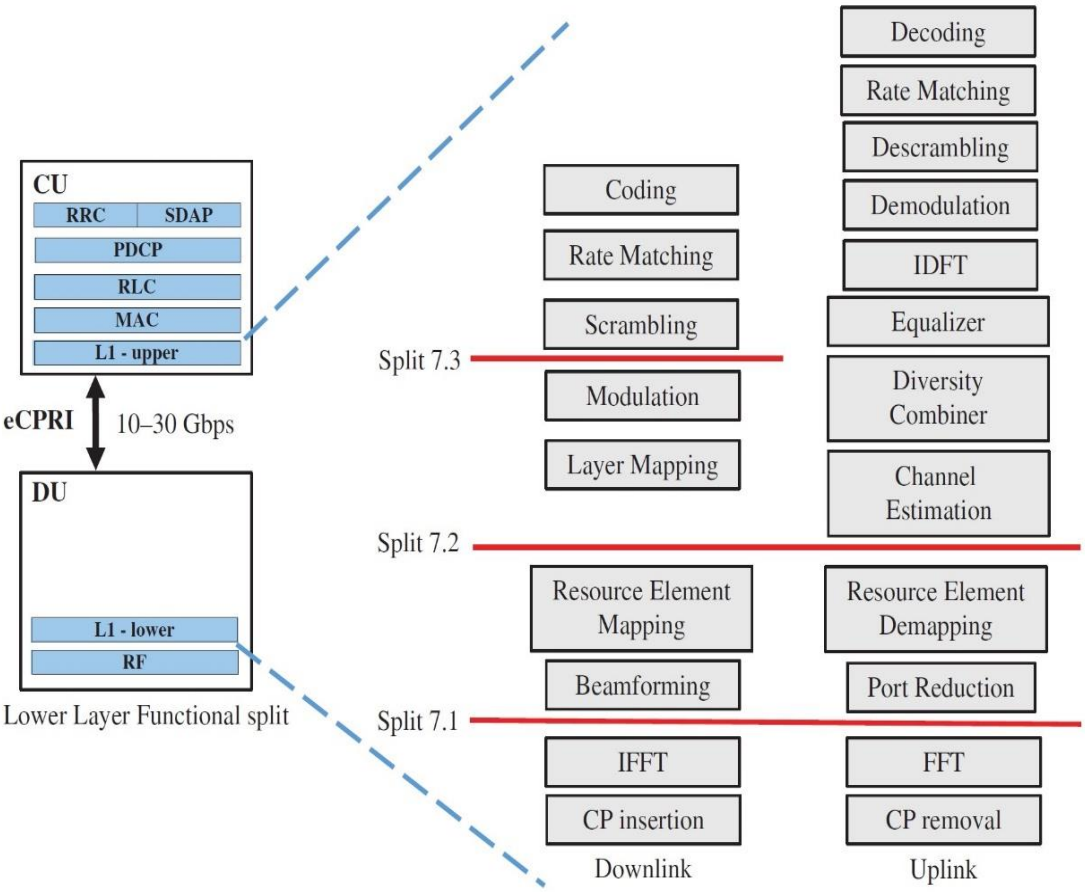


Fig.1. Options for Functional Partitioning 7 [19]

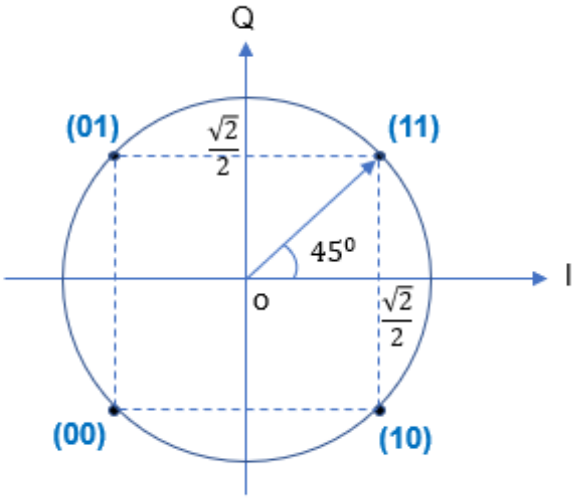
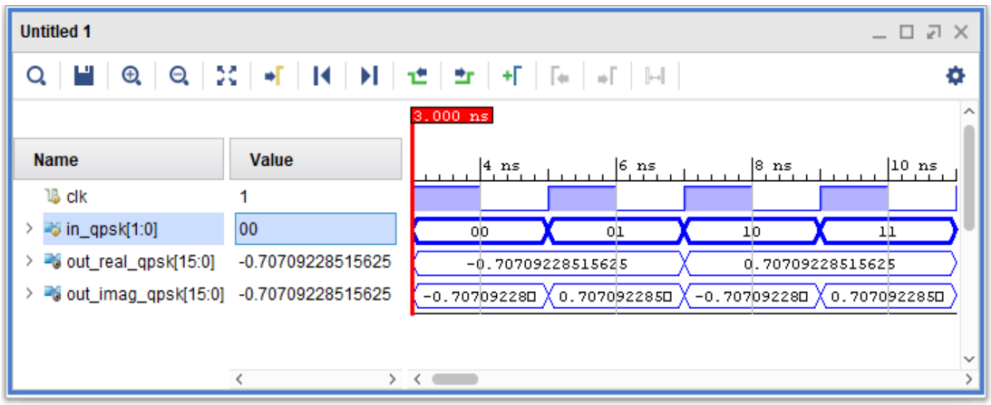
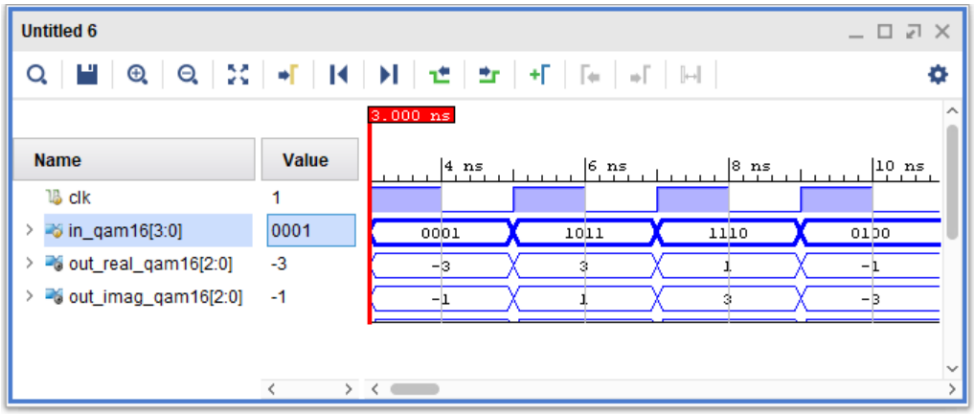


Fig.2. QPSK Constellations



(a)



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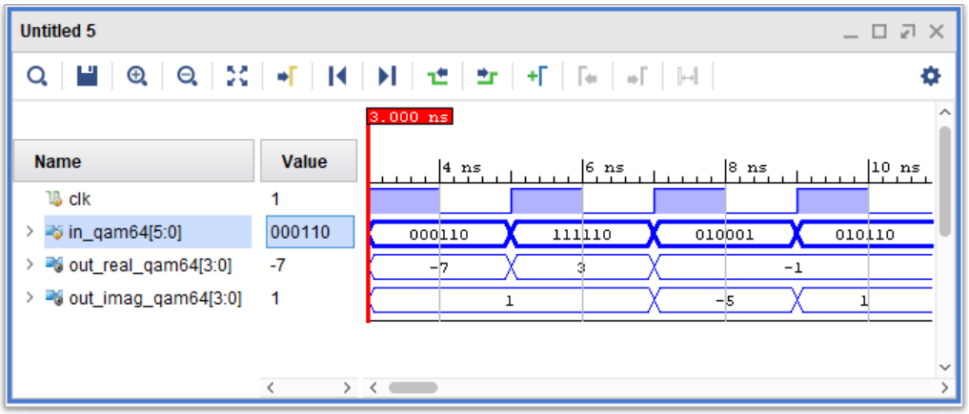
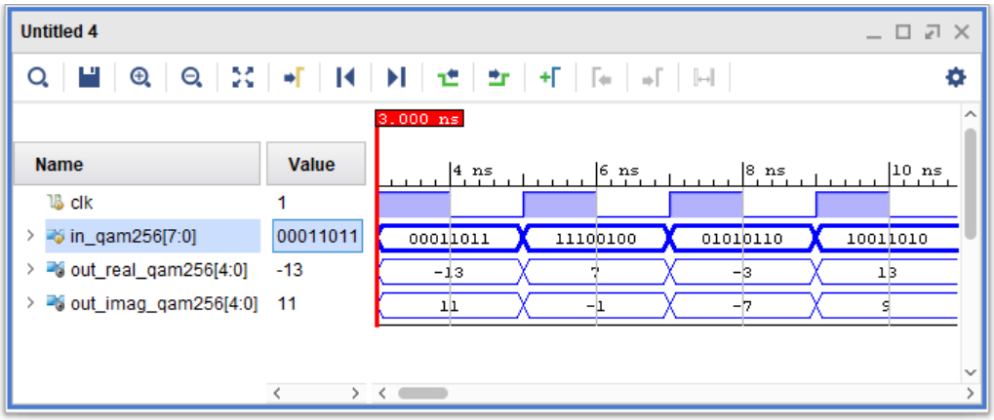


(c)



(d)

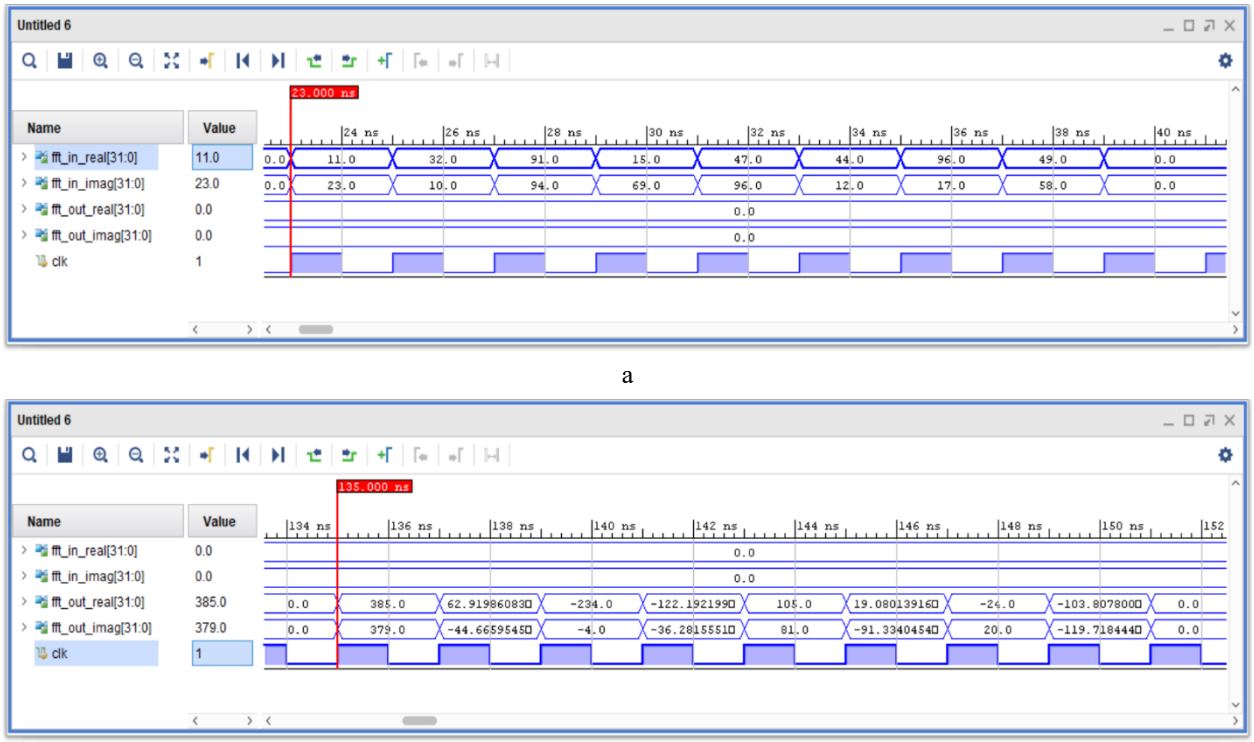
Fig.3. Results of …QPSK (a), 16QAM (b), 64QAM (c), 256QAM (d) Modulation for RU.

The execution time of this module is 0.01 microseconds at a frequency of 100 MHz. The resources utilized for the execution of this module are presented in Table 1. The results show that only the 256QAM modulation utilizes the BRAM (Block RAM) block, while the others utilize logical blocks. As the modulation complexity increases, the resources used also increase.

Table 1. FPGA Resource Utilization According to Modulation Types.

	QPSK	16QAM	64QAM	256QAM
LUT	2	2	4	0
FF	4	4	6	0
BRAM	0	0	0	1

However, QPSK and 16QAM exhibited identical resource utilization values. This could be attributed to the fact that QPSK employs fractional numbers, while 16QAM uses only integers. Additionally, a FFT/IFFT module was implemented, and the correctness of its operation was verified, as shown in Figure 4.



a

b

Fig.4. FFT Module Results for RU: (a) input data, (b) output data

The delay increases as the size of the transformation data grows. The results are shown in Figure 5 at a clock frequency of 100 MHz. However, the conversion frequency can be increased to 250 MHz. In that case, the delay time can be reduced by a factor of 2.5. The resources used for the execution of this module are presented in Figure 6.

It can be noted that the number of DSPs increases linearly with the growth of the transformation data size based on the obtained results of resource utilization. On the other hand, BRAM exhibits a non-linear dependence, meaning it increases exponentially with the growth of data size. This may be attributed to the fact that the computational complexity changes linearly while the memory used for computation increases exponentially.

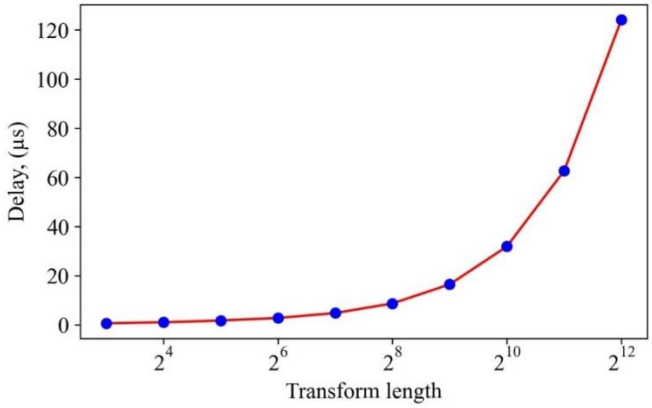


Fig.5. Dependence of Delay on FFT Module Size

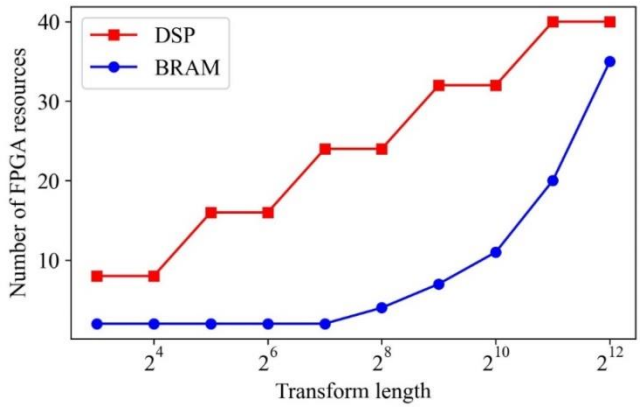


Fig.6. Dependence of FPGA Resources on FFT Module Size

5. Conclusion

In conclusion of this scientific work, it is noteworthy to highlight the successful implementation of a signal modulator supporting QPSK, 16QAM, 64QAM, and 256QAM on an FPGA platform using the Verilog programming language. The modulation results have confirmed the conformity of signal constellations and output data to theoretical expectations, emphasizing the reliability and efficiency of the proposed solution.

The execution time of the modulator was investigated, revealing a duration of 0.01 microseconds at a frequency of 100 MHz. Analysis of FPGA resource utilization allows for the identification of distinctive features associated with each modulation type, with resource consumption increasing in tandem with complexity. An interesting observation is that QPSK and 16QAM modulations exhibit identical resource usage, potentially explained by peculiarities in their numerical representations.

Additionally, an FFT/IFFT module was implemented and verified, featuring a delay dependent on the size of the transformation data. Increasing the transformation frequency can lead to a reduction in delay time. Resource utilization analysis also revealed that the number of DSP units increases linearly, while the usage of BRAM exhibits a nonlinear dependence, growing exponentially with the size of the data. This cautions against potential challenges related to memory volume in future expansions and optimizations.

Thus, the outcomes of this research not only affirm the effectiveness of implementing the FPGA-based modulator but also provide a foundation for further investigations into resource optimization and functionality expansion in communication systems.

Funding

This research was funded by the Committee of Science of Ministry of Science and Higher Education of the Republic of Kazakhstan, grant AP09058525.

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Article received 14.10.2023
Article accepted 22.11.2023